UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,420	12/11/2003	Winston Lee	MP0263	2013

44990 7590 11/27/2006

KENYON & KENYON LLP
333 W. SAN CARLOS STREET
SUITE 600
SAN JOSE, CA 95110-2731

EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,420	LEE ET AL.	
	Examiner	Art Unit	
	John P. Trimmings	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2006 and 03 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-21 and 23-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-21 and 23-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the applicant's RCE dated 11/3/2006 and amendment dated 10/13/2006.

The applicant has amended claims 1, 13 and 16.

Claims 1-6, 8-21 and 23-27 are pending.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/13/2006 has been entered.

Response to Amendment

2. Applicant's arguments with respect to claims 1-6, 8-21 and 23-27 have been considered but are moot in view of the new grounds of rejection (see below).

Claim Rejections - 35 USC § 102 (New)

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1- 4, 7-8, 13-19 and 22-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Heaslip et al. (herein Heaslip), U.S. Patent No. 6643807.

As per Claims 1 and 13 and 16:

Heaslip teaches a memory testing System/means and method based on the System comprising: a first memory tester (FIG. 1) with testing (FIG. 1 205, 210, 220, 230) and detecting means (FIG. 1 255) to detect failed location information from a memory (column 3 lines 12-13) at a first frequency (FIG. 1 BIST CLOCK 240/241); an interface (FIG. 1 206/251) in communication with the first memory tester (FIG. 1 lines 51-61); and a second memory tester (for example, column 4 lines 66-67), in communication with the interface (column 5 lines 33-39), which receives the failed location information at a second frequency (column 5 lines 66-67 and column 6 lines 1-12).

As per Claims 2 and 14 and 17:

Heaslip further teaches the memory testing system/method/means according to claim 1/13/16, wherein the first frequency is the memory operating frequency (column 6 lines 38-48).

As per Claims 3 and 15 and 18:

Heaslip further teaches the memory testing system/method/means according to claim 1/13/16, wherein the second frequency is the working frequency of the second memory tester (column 4 lines 26-39).

As per Claims 4 and 19:

Heaslip further teaches the memory testing system/means according to claim 1/16, wherein the first memory tester comprises a built-in self-test (see Abstract).

As per Claims 7 and 22:

Heaslip further teaches the memory testing system/means according to claim 1/16, wherein the first frequency is higher than the second frequency (column 2 lines 42-63).

As per Claims 8 and 23:

Heaslip further teaches the memory testing system/means according to claim 1/16, wherein the interface comprises a general processor input/output interface (column 3 lines 51-61).

Claim Rejections - 35 USC § 103 (New)

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 10, 11-12, 20 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaslip, as applied to claim 1 and 16 above, and further in view of Miner, U.S. Patent No. 6370661.

As per Claims 5 and 20:

Heaslip fails to further teach the memory testing system/means according to claim 1/16, wherein the first memory tester comprises a CPU. But in the analogous art of Miner, such a feature is taught in FIG.5 where a Configurable BIST uses microprocessor 501 for testing memory 1-4. Miner, in column 2 lines 8-25, the advantage is a configurable self test capability within a microprocessor for testing memories at full speed without excessive chip tester vector memory. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to incorporate the microprocessor control of Miner with the test system of Heaslip in order to decrease the chip tester vector overhead.

As per Claims 10 and 11 and 25 and 26:

Where Heaslip fails, Miner further teaches the memory testing system/means according to claim 1/16, wherein the second memory tester sends N clocks of data strobes at the second frequency to the interface upon detection of a failed memory location (column 10 lines 61-67 and column 11 lines 1-4). Described here in Miner is a well known process of scanning data out of the result register according to IEEE Standard 1149.1, where scanning, under control of a clock and TMS, is executed a fixed number of times (N) as required by the register size. And in view of the motivation previously stated, the claims are rejected.

As per Claims 12 and 27:

Heaslip further teaches the memory testing system/means according to claim 11/26, wherein the first memory tester asserts error (FIG.2 COMP STATUS) when a failed memory location is detected, and de-asserts error ("wait state", column 10 lines 44-48) before N-1 clocks of data strobes (FIG.5 188).

5. Claims 6 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaslip, as applied to claim 1 and 16 above, and further in view of Teh et al. (herein Teh), U.S. Patent No. 7010736.

As per Claims 6 and 21:

Heaslip fails to further teach the memory testing system/means according to claim 1/16, wherein the second memory tester comprises an external memory tester. But in the analogous art of Teh, such a feature is disclosed in column 3 lines 46-52 and column 4 lines 30-46. And Teh, in column 4 lines 30-46, the advantage is stated as being an arrangement that allows a memory tester to test many dies simultaneously with integrated BISTs in the DUT chips. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to incorporate the parallel test capabilities of Teh, including use of memory testers during test, with the test system of Heaslip in order to increase DUT chip test throughput.

6. Claims 9 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaslip, as applied to claim 1 and 16 above, and further in view of Au et al. (herein Au), U.S. Patent No. 6681359.

As per Claims 9 and 24:

Where Heaslip fails, Au further teaches the memory testing system/means according to claim 1/16, wherein the first memory tester asserts busy (RUN/TEST/IDLE, FIG.5 174) after receiving a test start signal (FIG.5 172). And in column 2 lines 18-26, the advantage is a test system that can test multiple memory devices with a single tester interface. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include the ideas of Au within the system of Heaslip, including memory busy identification so that many memories may be tested at once.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John P Trimmings
Examiner
Art Unit 2138

jpt